REMARKS

The Examiner has objected to the title of the specification as having the word "manufacturing" misspelled. The Examiner has also objected to claims 8-10 as substantially duplicative of claims 14-16.

The Examiner has rejected claims 8-11 and 14-17 under 35 U.S.C. 103 (a) over U.S. Patent 6067633 to Robbins, et. al. (hereinafter Robbins), in view of U.S. Patent 5,889,679 to Henry, et. al. (hereinafter Henry). The examiner has rejected claims 12-13 and 18-20 under 35 U.S.C. 103 over Robbins in view of Henry in further view of Microsoft Computer Dictionary (hereinafter MCD).

The Title.

Applicant has reviewed Examiner's objection to the title and states that the word "Manufacturing" is spelled correctly in Applicants' specification. Applicant attaches as Exhibit A a copy of the first page of the specification downloaded from the PAIR Website showing the correct spelling. Applicant also noted upon retrieval of Exhibit A that the title in PAIR is spelled incorrectly and requests that it be updated to reflect the correct title.

The New Claims

New Claim 21 is derived from old claims 8 and 10, with the types of functional units more explicitly defined. These functional units are smaller portions of a processor integrated circuit or computer system than the processors or complete caches of Robbins.

As stated in paragraph 30 of the present application, when at least one functional unit of each processing type (such as floating point processing units and integer processing units) remains active, the processor retains the ability to execute all instructions of its instruction set. This differs from the Henry reference, in that Henry sacrifices instruction set compatibility when he disables the only MMX unit on his processor.

New claim 22 drops branch prediction units from the list of functional units that may be disabled.

New claim 23 is derived from old claims 14 and 15. Neither Henry nor Robbins discloses looking up performance in a performance table. While the

Examiner cited Column 3, lines 44 to 57, of Robbins for this element, Robbins does not actually mention a table anywhere. Further, neither Henry nor Robbins disclose preparing a performance table by using benchmark results.

When a processor loses (for example but not by way of limitation) one of two floating point processing units, the impact on performance is not always easily predictable because application programs have a mix of instructions that varies with application type. Some applications, such as word processors, may be impacted slightly, others, such as Spice-like circuit simulators, may suffer significant impact. Similarly, loss of one of three integer processing units may have a much greater effect on a database program than on a highly floating-point oriented circuit simulator.

A way of classifying performance of a processor having a subset of functional units is to run a variety of application programs on the processor. Unfortunately that is not practical in volume production. Alternatively, and as claimed, applications can be benchmarked for a variety of configurations. Performance classifications derived from those benchmarks are stored in a table; performance is quickly determined during manufacturing by lookup of the configuration of enabled units for each processor in that table.

New claim 24 attempts to capture the essence of the reject signal described in paragraphs 43 and 44 of the application. Reject signals are not described in the cited art.

The Cancelled Claims

Claims 8, 10, 14, 15 are cancelled. Claims 1-7 were withdrawn as not elected in response to a restriction requirement.

The Amended Claims

Claims 11 to 13 have been amended to depend on new claims 21 or 22; and are patentable if their parent claim is patentable. Similarly with claims 19 and 20.

Claim 17 has also been amended to depend on new claim 23, as with claims 16 and 18.

Claim 17 adds to parent claim 23 the element of determining enabled and disabled functional units based upon the results of a built-in self test (BIST) performed on powerup of the integrated circuit. The Examiner relied on Henry for

this element in his rejection. While Henry discusses disabling functional units after manufacture in the context of "per manufacturer's instructions due to problems in certain environments ", this is very different from built-in self test. Nowhere in Henry or Robbins does any reference to BIST occur.

The Examiner relied on Microsoft Computer Dictionary for the element of enabling or disabling a branch prediction unit associated with claims 12, 13, and 18-20. As the examiner stated, a branch prediction unit enhances performance, so processors lacking a branch prediction unit would have lower performance and price than those with such a unit. Applicant notes that processors designed to perform speculative execution and to make use of a branch prediction unit in their control logic are generally scrapped rather than sold when the branch prediction unit is defective because the processor as a whole is designed such that the prediction unit is required for normal operation. Nowhere in the cited references is it suggested that a branch prediction unit can be disabled while leaving a functional integrated circuit.

Conclusions

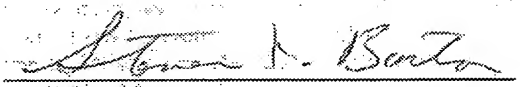
Applicant respectfully requests that the Examiner reconsider the amended claims in light of the foregoing remarks.

Applicant believes no fees are currently due, however, if any fee is deemed necessary in connection with this Amendment and Response, please charge Deposit Account No. 08-2025.

Respectfully submitted,

LATHROP & GAGE L.C.

Date: June 29, 2005

By: 

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METHOD AND APPARATUS FOR IMPROVING YIELD BY DECOMMISSIONING OPTIONAL UNITS ON A CPU DUE TO MANUFACTURING DEFECTS

FIELD OF THE INVENTION

[0001] The invention pertains to the field of design and packaging of large, complex, integrated circuits such as processors. In particular, the invention relates to a method of design and packaging CPU integrated circuits so that partially-defective processor circuits may be sold as reduced-performance processor circuits.

BACKGROUND OF THE INVENTION

[0002] It is well known in the art of integrated circuits that manufacturing processes are imperfect – on each wafer some, but not all, integrated circuits function fully. It is also known that defects tend to occur in clusters. Therefore, for circuits having multiple, large, functional units, there will be a substantial population of manufactured integrated circuits where one functional unit is defective, or even a small portion of a functional unit is defective, but other functional units on the same integrated circuit function properly.

[0003] The probability that an integrated circuit will have one or more defects increases as the size of the integrated circuit increases. Further, the cost of fabrication increases as integrated circuit size increases. A high performance single or multiple-processor integrated circuit can be quite large. It is therefore desirable to find ways of selling at least some of those integrated circuits that contain one or a few defects.

[0004] Typically, integrated circuits are tested before they are packaged. Those processor circuits that have defective units are often discarded before packaging; their fabrication cost is wasted but further investment in them is prevented.

[0005] Solutions that permit selling partially-defective integrated circuits are known for memory integrated circuits. For example, memory integrated circuits often have spare blocks of memory that can be substituted for defective sections of the circuit. Before spare blocks became common, memory circuits were occasionally packaged with a high-order address bit wirebonded to a constant, then sold as memories of half capacity, with defective sections of the chip disabled. Wirebonding a bondpad to a constant to configure an integrated circuit is known as a bonding option; bonding options may also be implemented through a package trace where a particular package lead is tied to a

Exhibit A